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10/762,037	01/29/2004	Zohar Bogin	42P18575	3941
59796 7590 10/29/2008 INTEL CORPORATION c/o INTELLEVATE, LLC P.O. BOX 52050 MINNEAPOLIS, MN 55402				
EXAMINER SUN, SCOTT C				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/762,037  
Filing Date: January 20, 2004  
Appellant(s): BOGIN ET AL.

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Intel Corporation  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 7/30/2008 appealing from the Office action mailed 7/24/2007.

Application/Control Number: 10/762,037  
Art Unit: 2182

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**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

Patent Application Publication 2003/0177296	Kurth	09-2000
Patent Application Publication 2003/0210710	Odman	11-2003
Patent Application Publication 2002/0116555	Somers	08-2002

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurth (PG PUB # US2003/0177296).

Regarding claim 1, Kurth discloses a method (method shown in figures 4) comprising:

dynamically modifying one or more attributes (select priority level; step 400) of each of a plurality of requests (work requests from the multiple agents shown in figure 1) to access one or more memory devices (SRAM or FIFO; paragraph 15), wherein dynamically modifying the one or more attributes comprises dynamically prioritizing (changing the priority level of the request) the plurality of requests in response to latency sensitivity (relative wait time of the requests, or waiting timer) of each of the plurality of requests (methods shown in figures 5A and 5B; detail in paragraphs 22, 23, waiting timer shown in figure 6, details in paragraph 25); and

arbitrating among the plurality of requests to select a request to send to the one or more memory devices in a time slot based on the one or more attributes (step 402, 404; paragraph 21);

Regarding claim 3, Kurth discloses the method of claim 2, and further discloses wherein the latency sensitivity of each of the plurality of requests changes in response to space available in a buffer storing the corresponding request (paragraph 22 and 23).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurth further in view of Odman (PG Pub # US2003/0210710).

Regarding claim 4, Kurth discloses various elements as shown in rejection of claims 1, but does not disclose explicitly dynamically changing lengths of the requests. However, Odman discloses combining multiple requests (frames or fragments) into a larger request (a burst transfer) to fill a given time slot (paragraphs 93, 97). Teachings of Kurth and Odman are from the same field of data transmission, and specifically of transfer scheduling.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Kurth and Odman by combining multiple

smaller requests into larger requests to fill time slots for the benefit of reducing wasted bandwidth (paragraph 93).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurth in view of applicant's admitted prior art (APA).

Regarding claims 5 and 6, Kurth discloses claim 1, but does not disclose explicitly the request types. However, applicant's admitted prior art discloses the requests can be read, write or buffer descriptor read requests (memory access requests according to the PCI Express protocol, which includes data read, data write, and buffer descriptor read requests). Teachings of Kurth and applicant's admitted prior art are from the same field of data transfers between computer components, and specifically of scheduling requests.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Kurth and APA by using the method disclosed by Kurth in a PCI Express protocol environment for the benefit of fair request arbitration (paragraph 7, Kurth; paragraph 4, APA).

Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurth in view of Somers et al (PG Pub # US2002/0116555).

Regarding claim 7, Kurth discloses claim 1 but does not disclose explicitly a plurality of DMA controllers. However, Somers discloses a plurality of DMA controllers

for handling data transfers (paragraph 3). Teachings of Somers and Kurth are from the same area of data transmissions between computer components.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Kurth and Somers by using a plurality of DMA controllers to assert access requests for the benefit of efficient data transfer (paragraph 3, Somers).

## **(10) Response to Argument**

### **I. Claim 1**

#### **Issue I – 102 rejection**

Appellant argues that the prior art of record, Kurth, does not disclose the claim limitation “dynamically modifying one or more attributes of each of a plurality of requests to access one or more memory devices, wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests”.

#### **Examiner's Response to the Issue**

Examiner notes that appellant argues that the cited portion of the prior art, specifically paragraph 21 of Kurth, does not disclose the above limitation. However, in the final rejection regarding the above limitation, examiner cited paragraphs 22, 23, and 25, as well as figures 5A and 5B. In fact, paragraph 22 specifically teaches a “dynamic request priority algorithm” that “dynamically increase the priority level of priority requests



as the request queue fills up" to "ensure that the agent is not starved for access to the resource" (last six lines of paragraph 22). The rejection further cites paragraph 25, in which a "timer" is used to "determine if the priority request is granted before the timer expires. If access has not been granted before the timer expires, the agent increases the priority level of the request". So the longer a request has been waiting, the increasing higher its urgency, or latency sensitivity, and correspondingly is assigned a higher priority level. Therefore, it is clear that the requests are modified based on their latency sensitivity as well.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Scott Sun

Patent Examiner

Art Unit 2182

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